What is claimed is:

1. A disk drive control system comprising:

a micro-controller;

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller;

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory; and

a cache demand circuit adapted to:

a) receive a memory address and a memory access signal, and

b) cause the micro-controller cache system to fetch data from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request.

2. The disk drive control system of claim 1, wherein the memory address and a memory access signal are received from the micro-controller and wherein the memory address is an address of data residing in the remote memory.

3. The disk drive control system of claim 1, wherein the memory access signal is a write signal received from the micro-controller.

4. The disk drive control system of claim 1, wherein the memory access signal is a priority interrupt signal.

5. The disk drive control system of claim 4, wherein the memory address is a predetermined memory address received prior to the memory access signal.

6. The disk drive control system of claim 5, wherein the cache demand circuit is further adapted to store the predetermined memory address of data residing in the remote memory.

7. The disk drive control system of claim 6, wherein the received interrupt signal causes the cache demand circuit to provide the predetermined memory address to the micro-controller cache system for fetching of data from the remote memory via the buffer manager.

8. The disk drive control system of claim 7, wherein the fetched data are accessed from the micro-controller cache system by the micro-controller during a micro-controller interrupt service routine.

9. The disk drive control system of claim 5, wherein the cache demand circuit is adapted to store the predetermined memory address of the data in a cache demand circuit register.

10. The disk drive control system of claim 1, wherein the micro-controller cache system comprises a cache memory having a plurality of cache segments wherein the fetched data is stored in a cache segment of the memory.

11. The disk drive control system of claim 1, wherein the micro-controller cache system is adapted to receive the memory address and the memory access signal from the cache demand circuit.

12. The disk drive control system of claim 1, wherein the buffer manager is in communication with a plurality of control system clients and provides client-requested data to the clients from the remote memory.

13. The disk drive control system of claim 12, wherein the plurality of control system clients comprises at least one of a disk subsystem, an error correction code subsystem, and a host interface subsystem.

14. The disk drive control system of claim 1, wherein the remote memory comprises a dynamic random access memory (DRAM).

15. The disk drive control system of claim 4, wherein the memory access signal is a servo-interrupt signal.

16. The disk drive control system of claim 4, wherein the memory access signal is a host-interrupt signal.

17. A disk drive control system comprising:

a micro-controller;

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller;

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory; and

a cache demand circuit adapted to:

a) receive a memory address and a memory access signal from the micro-controller, and

b) cause the micro-controller cache system to fetch data from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request.

18. A disk drive control system comprising:

a micro-controller;

a micro-controller cache system adapted to store micro-controller data for access by the micro-controller;

a buffer manager adapted to provide the micro-controller cache system with micro-controller requested data stored in a remote memory;

an interrupt circuit adapted to interrupt the micro-controller based on a transmitted interrupt signal; and

a cache demand circuit adapted to:

a) receive a predetermined memory address from the micro-controller and the transmitted interrupt signal from the interrupt circuit, and

b) because the micro-controller cache system to fetch data from the remote memory via the buffer manager prior to a micro-controller request.

19. The disk drive control system of claim 18, wherein the received transmitted interrupt signal causes the cache demand circuit to provide the predetermined memory address of data in the remote memory to the micro-controller cache system, wherein the micro-controller cache system fetches the data from the remote memory via the buffer manager.

20. The disk drive control system of claim 19, wherein the predetermined memory address is received in the cache demand circuit prior to the transmitted interrupt signal.